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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/754,926	01/04/2001	Kie Y. Ahn	MI22-1533	3846
21567	7590	02/18/2005	EXAMINER	
WELLS ST. JOHN P.S. 601 W. FIRST AVENUE, SUITE 1300 SPOKANE, WA 99201			KIELIN, ERIK J	
			ART UNIT	PAPER NUMBER
			2813	

DATE MAILED: 02/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/754,926	AHN ET AL.	
	Examiner	Art Unit	
	Erik Kielin	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 01 December 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 3,5,6,8-10 and 31-33 is/are pending in the application.
- 4a) Of the above claim(s) none is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 3,5,6,8-10 and 31-33 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

This action responds to the Amendment filed 1 December 2004.

Election/Restrictions

It is noted that Applicant has amended independent claim 10 to incorporate the limitation, "implanting a conductivity-enhancing dopant into the substrate through the layer of Al₂O₃-doped with silicon atoms." Applicant elected the species of Group I, drawn to the formation of a silicon-doped aluminum oxide layer on a substrate. (See election filed 25 October 2001.) The implantation is considered drawn to the non-elected species of Groups II and III because the implantation step has nothing to do with forming the silicon-doped aluminum oxide layer. While the claims will be examined presently, Applicant is admonished that should any further features drawn to the non-elected species of Groups II and III, be added to the instant claims, the claims may be subject to restriction by original presentation. Any claims drawn to the species of Groups II and III may be withdrawn from consideration as being drawn to non-elected species.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 10, 3, 5, 6, 8, 9, 31, and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 5,923,056 (Lee et al.) in view of the basic text of Vossen and Kern, Thin

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Film Processes II, Academic Press: Boston, 1991, pp. 80-81, 108-110, 113-115, 188, 200 and JP 60-167352 A (**Fujisada**) and Wolf, et al. Silicon Processing for the VLSI Era, Vol. 1-Process Technology, Lattice Press: Sunset Beach CA, 1986, pp. 5 and 323 (**Wolf-1**), and Silicon Processing for the VLSI Era, Vol. 2-Process Integration, Lattice Press: Sunset Beach CA, 1990, pp. 354-356 (**Wolf-2**).

Regarding independent claim 10, Lee discloses forming a variety of semiconductor devices including MOSFET, flash EPROM, capacitors, DRAMs, etcetera (i.e. "an assembly" comprising a doped metal oxide, which may be a silicon-doped porous aluminum oxide (col. 1, line 66 to col. 2, line 10; col. 3, lines 19-40; col. 4, first paragraph) comprising:

an exemplary method disclosed at cols. 5-6, "EXAMPLE 1", wherein the silicon-doped aluminum oxide layer **18** is formed on a semiconducting material ("silicon wafer **110**") by sputtering (i.e. evaporating) from a target containing aluminum with 1% silicon (i.e. evaporating silicon and aluminum) in a chamber having argon and oxygen, wherein sputtering/evaporation is generated by glow discharge plasma;

the evaporated silicon and aluminum react with oxygen to form evaporated silicon oxide and aluminum oxide, which mix and deposit as silicon-doped porous aluminum oxide **18** on the silicon semiconductor wafer **110**; and

forming a conductive material (called the "gate **13**" in Lee) over the insulating layer silicon-doped porous aluminum oxide **18**, the conductive material **13** being separated from the semiconductive material **110** by the silicon-doped porous aluminum oxide layer **18**. (Figs. 1 and 2).

Lee does not disclose that specifically silicon monoxide and aluminum oxide in the form of sapphire are evaporated from separate sources, but does expressly state that the doped metal oxide films, such as the exemplary silicon-doped aluminum oxide film, may be formed using “a conventional deposition technique such as sputtering ...” (col. 2, lines 15-21).

The basic textbook of **Vossen and Kern** teaches conventional techniques for forming thin films including forming a mixed or alloy film using “two-source sputtering, with one source for one alloy component and the other source for the second component.” (See p. 200, section entitled “*Targets*.”) **Vossen and Kern** also teaches numerous examples of mixed composition films formed using separate evaporative sources on pages 108-109, Table II which form a vapor mixture to form the mixed composition layer made from the separate evaporative sources. Sources for aluminum oxide (Al_2O_3) and silicon monoxide (SiO) are also taught to be known, on pages 113-115, Table III, as well as the composition of the vapor upon evaporation of a given source. Note in pertinent point that both SiO and SiO_2 provide SiO as the main component of the vapor. So even if SiO_2 is thermally evaporated, SiO is the vapor species formed, and oxygen from SiO or SiO_2 is necessarily incorporated into the deposited film because SiO is necessarily incorporated into the deposited film. **Vossen and Kern** also teaches that the deposition rate of each component (e.g. the SiO and the Al_2O_3) must be separately controlled to ensure that the composition of the deposited layer reflected that desired. In this regard, **Vossen and Kern** states at p. 110, under the section entitled, “Co-evaporation Using Multiple Source[s]”

“In elaborate systems, separate deposition monitors are used with appropriate feedback networks to **control the deposition rate from each individual source independently**. Near-stoichiometric film of many binary alloys have been deposited using this technique.”
(Emphasis added.)

Vossen and Kern also teach that no additional oxygen is added if the source materials themselves have oxygen in them already (Table II, p. 108 where no additional oxygen is fed in during the deposition of Cr-SiO composite films).

It would have been obvious to one of ordinary skill at the time of the invention to use a silicon monoxide source and an aluminum oxide source with controlled evaporation rate and without additional oxygen fed into the reactor to form a silicon-doped aluminum oxide film with the desired amount of silicon, because the choice of SiO and Al₂O₃ sources are well known and will result is the same silicon-doped aluminum oxide as that disclosed in **Lee**, and because **Lee** teaches “a **conventional** deposition technique such as sputtering” will work, and because the use of separate sources with controlled deposition rate to form a mixed or alloy layer of the desired composition of each component is **conventional**, as taught by **Vossen and Kern**.

It would have been obvious for one of ordinary skill in the art, at the time of the invention to preclude O₂ from flowing into the chamber during the evaporation, mixing and deposition of the SiO and Al₂O₃ in **Lee**, since each of SiO and Al₂O₃ already provide oxygen, such that no additional oxygen is necessary, as taught in **Vossen and Kern** (Table II, p. 108 where no additional oxygen is fed in during the deposition of Cr-SiO composite films and Table III, p. 113 which shows that Al₂O₃ decomposed to produce O and O₂ upon evaporation). Further in this regarding, the specification states that oxygen can be precluded from the chamber. Accordingly, there exists no criticality to the presence or absence of oxygen.

*Applicant could overcome the rejection by providing evidence that the specific use of silicon monoxide and aluminum oxide provides unexpected results in the Si-doped aluminum oxide film relative to that source used in **Lee**.* Presently there is no such evidence of record.

Lee and Vossen and Kern do not indicate that sapphire is the aluminum oxide source.

Fujisada teaches the benefits of preventing injurious impurities from being incorporated into sputter-deposited aluminum oxide films by using a sapphire target, specifically for use in semiconductor device applications. (See Abstract.) Note that sapphire is necessarily single crystal because that which distinguishes aluminum oxide from sapphire is *only* the fact that sapphire is a single crystal of aluminum oxide.

It would have been obvious to one of ordinary skill at the time of the invention to use a sapphire source as the aluminum oxide source in the method of **Lee** in view of **Vossen and Kern** to prevent contamination of the deposited film, as taught by **Fujisada**.

Then the only difference is drawn to the method of manufacture the source/drain regions, specifically by implantation of dopants (either n-type or p-type) through the Si-doped aluminum oxide gate dielectric.

Wolf-2 teaches conventional methodology for fabricating a MOSFET (such as that indicated by **Lee** to be conventional) wherein the source/drain regions are formed by implantation of either n-type or p-type dopants through the gate oxide insulating layer. (See **Wolf-2**, at pages 354-356; section entitled, "5.6.5 Lightly Doped Drains" particularly Figs. 5-30 process steps (a) and (f) and Table 5.2 the columns labeled "Twin-Tub V" and "Twin-Tub VI.") Additionally, **Wolf-1** at page 323 teaches the implantation through a thin oxide layer has two main benefits: (1) to act as a screen against impurities that would otherwise be introduced by the implantation processing, and (2) to reduce channeling of implanted ions.

It would have been obvious for one of ordinary skill in the art, at the time of the invention to follow the conventional method of **Wolf-2** to implant the source/drain regions through the gate

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oxide layer in the transistor of **Lee**, because **Lee** teaches that the MOSFET fabrication is **conventional** and **Wolf-2** shows that implantation through the gate oxide layer is **conventional**, and because **Wolf-1** teaches that the oxide layer prevents contamination during implantation while preventing channeling of implanted ions. Moreover, one of ordinary skill would recognize that the gate oxide layer use as a protective layer provides dual use to the layer and thereby prevents the removal of the gate oxide over the source/drain regions and formation distinct protective layers to prevent contamination and ion channeling.

Regarding claim 3, 5, and 6, **Lee** does not specifically indicate that the evaporation means is thermal evaporation, but **Vossen and Kern** teach the thermal evaporation is one of the art-recognized equivalent means of evaporating a source material to deposit a film. (See **Vossen and Kern**, p. 80, second sentence under section entitled "Evaporation Process.") **Vossen and Kern** also teach that evaporation is conventionally carried out using, *inter alia*, electron beams (guns) (pp. 80-81), and that ion beams are conventionally used for sputter deposition (p. 188).

It would have been obvious for one of ordinary skill in the art, at the time of the invention to use thermal evaporation, electron beams (guns), or ion beams as the method of evaporating sapphire, as taught by **Lee** in view of **Vossen and Kern** and **Fujisada**, because **Vossen and Kern** teach that each evaporation means is an art known means in which to evaporate a source to deposit a film. Moreover, there is no evidence of record that thermal evaporation provides some unexpected results relative to the other methods. Rather the evidence of record teaches away from any unexpected result since plural methods are indicated in the specification and claimed as being usable for evaporating the aluminum oxide source, whether it is sapphire or just aluminum oxide.

Regarding claim 8, **Lee** discloses the silicon substrate (col. 5, line 56).

Regarding claim 9, **Lee** does not specifically state that the silicon substrate is “monocrystalline.”

Wolf-1 teaches that integrated circuits are formed on monocrystalline or “single crystal” silicon substrates (p. 5, first paragraph under section entitled “Manufacture of Single Crystal Silicon.”)

It would have been obvious to one of ordinary skill at the time of the invention to use the notoriously well-known monocrystalline substrates as the silicon substrate of **Lee**, because **Wolf** teaches that monocrystalline is always used over other forms of silicon to enable sufficient carrier lifetime in semiconductor devices.

Regarding claim 31, **Lee** specifically states that the dopant is 0.1 to 30 weight percent of the dielectric film. (See Abstract.)

Regarding claim 32, **Lee** teaches an exemplary embodiment where the substrate temperature is 380 °C, but does not indicate that the semiconductor material is at room temperature during the deposition.

Vossen and Kern teach several examples of forming doped metal oxides using and SiO target, for example, wherein the temperature range of the substrate is 25-300 °C. (See Table II.)

It would have been obvious for one of ordinary skill in the art, at the time of the invention to deposit the silicon-doped aluminum oxide of **Lee** at room temperature, because **Lee** teaches conventional sputtering methods may be used and **Vossen and Kern** teaches that sputtering at room temperature is conventional for doped oxide formation. Furthermore, it would be a matter of routine optimization to sputter deposit the silicon-doped aluminum oxide at room temperature

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because it is a matter of determining optimum process condition by routine experimentation with a limited number of species. See *In re Jones*, 162 USPQ 224 (CCPA 1955)(the selection of optimum ranges within prior art general conditions is obvious) and *In re Boesch*, 205 USPQ 215 (CCPA 1980)(discovery of optimum value of result effective variable in a known process is obvious). One of ordinary skill would be especially motivated to use room temperature since **Vossen and Kern** teach that this temperature is conventional and in order to reduce the thermal budget which enables the production of smaller device features without fear of diffusion or damaging previously formed device features.

3. Claim **33** is rejected under 35 U.S.C. 103(a) as being unpatentable over US 5,923,056 (**Lee et al.**) in view of the basic text of **Vossen and Kern**, Thin Film Processes II, Academic Press: Boston, 1991, pp. 80-81, 108-110, 113-115, 188, 200.

Lee discloses forming a variety of semiconductor devices including MOSFET, flash EPROM, capacitors, DRAMs, etcetera (i.e. “an assembly) comprising a doped metal oxide, which may be a silicon-doped porous aluminum oxide (col. 1, line 66 to col. 2, line 10; col. 3, lines 19-40; col. 4, first paragraph) comprising:

an exemplary method disclosed at cols. 5-6, “EXAMPLE 1”, wherein the silicon-doped aluminum oxide layer **18** is formed on a semiconducting material (“silicon wafer **110**”) by sputtering (i.e. evaporating) from a target containing aluminum with 1% silicon (i.e. evaporating silicon and aluminum) in a chamber having argon and oxygen, wherein sputtering/evaporation is generated by glow discharge plasma;

the evaporated silicon and aluminum react with oxygen to form evaporated silicon oxide and aluminum oxide, which mix and deposit as silicon-doped porous aluminum oxide **18** on the silicon semiconductor wafer **110**; and

forming a conductive material (called the “gate **13**” in **Lee**) over the insulating layer silicon-doped porous aluminum oxide **18**, the conductive material **13** being separated from the semiconductive material **110** by the silicon-doped porous aluminum oxide layer **18**. (Figs. 1 and 2).

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incorporated into the deposited film. **Vossen and Kern** also teaches that the deposition rate of each component (e.g. the SiO and the Al₂O₃) must be separately controlled to ensure that the composition of the deposited layer reflected that desired. In this regard, **Vossen and Kern** states at p. 110, under the section entitled, "Co-evaporation Using Multiple Source[s]"

"In elaborate systems, separate deposition monitors are used with appropriate feedback networks to **control the deposition rate from each individual source independently**. Near-stoichiometric film of many binary alloys have been deposited using this technique."
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additional oxygen is fed in during the deposition of Cr-SiO composite films and Table III, p. 113 which shows that Al_2O_3 decomposed to produce O and O_2 upon evaporation). Further in this regarding, the specification states that oxygen can be precluded from the chamber. Accordingly, there exists no criticality to the presence or absence of oxygen.

Response to Arguments

4. Applicant's arguments with respect to claims 10, 3, 5, 6, 8, 9, 31, and 32 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

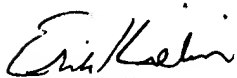
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Erik Kielin whose telephone number is 571-272-1693. The examiner can normally be reached from 9:00 - 19:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr. can be reached on 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Erik Kielin
Primary Examiner
February 17, 2005